

REMARKS

This is in response to the Office Action dated September 17, 2004, and the references cited therewith.

Claim 7 is amended. Claims 7-13 and 20-25 are pending.

Drawings

The drawings were objected to for not showing each feature specified in the claims. The Office Action states that Fig. 3 does not show the chip being connected to the circuit board. Applicant notes that Figure 5 shows a chip 526 mounted to circuit board 532. The Office Action further states that Fig. 3 or 5 does not show the leadframe connecting the chip to the board such that the electrical component is mounted on/above the major surface of the IC chip. Applicant again notes that Fig. 5 shows TAB structure 400 connecting chip 526 to circuit board 532 such that an electrical component 504 is mounted above the major surface of the IC chip 526.

Reconsideration of the drawing objections is respectfully requested.

§103 Rejection of the Claims

Claims 7, 9, 11, 12, 20-22, 24 and 25 were rejected under 35 USC § 103(a) as being unpatentable over Takeda et al. (U.S. Patent No. 5,892,271) in view of Bickford et al. (U.S. Patent No. 4,862,322).

Claims 7, 9, and 20-22

Applicant has amended claim 7 to better describe the subject matter recited in the claim. Applicant believes claim 7 is not obvious in view of the cited references since, even if combined, the combination does not include each limitation recited in the claim. For example, Applicant cannot find in the combination an electrical component mounted on or above a surface of the IC chip and electrically connected to the IC chip via a lead on the TAB leadframe which extends outward from the electrical component to a perimeter I/O of the IC chip, as recited in claim 7. In contrast, Takeda does not discuss such subject matter at all and Bickford discusses a double-device structure where the devices are both coupled at their perimeters to an ILB end 38 of a leadframe. (See Fig. 2 of Bickford). Accordingly, the cited

references in combination do not include a lead on the TAB leadframe which extends outward from the electrical component to a perimeter I/O of the IC chip, as recited in claim 1.

Claims 9 and 20-22 include each limitation of their parent claim and are therefore not obvious in view of the cited references. Reconsideration and allowance is respectfully requested.

Claims 11, 12, 24, and 25

Applicant traverses the rejection of claims 11, 12, 24, and 25 since, even if combined, the combination does not include each limitation recited in the claim. Moreover, there is no suggestion to combine the references.

The reference (or references when combined) must teach or suggest all the claim elements. M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)). Claim 11 recites an electrical device including a TAB leadframe connecting the IC chip to the circuit board, the TAB leadframe including a plurality of leads, a first area of the plurality of leads configured into a generally rectangular ILB portion which is dimensioned to directly connect one or more of the plurality of leads to the perimeter I/Os of the IC chip, a second area of the plurality of leads configured into an OLB portion for connecting one or more of the plurality of leads to the circuit board, wherein at least one of the plurality of leads is internally routed relative to the ILB area so that the at least one lead has a contact exposed interior to the ILB portion of the TAB structure and above a major surface of the IC chip. Applicant cannot find such subject matter in either reference, either singly or in combination.

The Office Action asserts that Takeda includes “a plurality of leads (see 8 in Fig. 3 and 10), the leads having a first area of the plurality of leads being internally routed and configured into an inner lead bonding (ILB) area/portion and an outer lead bonding (OLB) area/portion having external electrodes (see 6 in Fig. 3; Col. 4, line 7)) ... [and] the ILB portion of the leads having terminals/contacts being exposed (see 7 in the ILB portion under the IC chip in Fig. 3).” (Page 4 of the Office Action). However, Takeda discusses that metal projection bumps 7 are formed on electrodes 6. (See col. 4, lines 3-6). Accordingly, they cannot be both the ILB and the OLB as defined by the Office Action. Accordingly, if the Office Action is saying that bumps 7/electrodes 6 are an OLB portion, then Takeda does not include at least one of the plurality of leads internally routed relative to the ILB area, as recited in the claim. If the Office Action is

saying that bumps 7/electrodes 6 are an ILB portion, then such a structure does not include an ILB portion that directly connects one or more of the plurality of leads to the perimeter I/Os of the IC chip, as recited in the claim. Accordingly, neither interpretation includes the subject matter recited in the claim. As noted above, the secondary reference, Bickford, also does not include such subject matter.

Moreover, Applicant notes that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Here, there is no motivation to make the asserted modification to the primary reference. Takeda discusses mounting an IC 1 to a PCB 18 via a substrate 4 (see Fig. 4, for example). Takeda shows contacts 2 facing the PCB 18. Bickford discusses a package of devices mounted with active faces placed facing each other to form a double-device structure. (Abstract, Bickford). In Bickford, the back of the bottom device faces the PCB. Accordingly, modifying Takeda into a double-device package would not be logical. Such a modification would not allow the Takeda chip to be mounted directly to the PCB 18 since Takeda shows contacts 2 facing the PCB 18 with no room for mounting another device between the IC 1 and the PCB 18.

Claims 12, 24, and 25 include each limitation recited in their parent claim and are therefore also not obvious in view of the cited reference. Reconsideration and allowance is respectfully requested.

Claims 8 and 23 were rejected under 35 USC § 103(a) as being unpatentable over Takeda et al. (U.S. Patent No. 5,892,271) and Bickford et al. (U.S. Patent No. 4,862,322) as applied to claim 7 above, and further in view of Buckley, III et al. (U.S. Patent No. 5,477,082). Claims 8 and 23 include each limitation of their parent claim and are therefore not obvious in view of the cited references since the secondary reference does not overcome the deficiencies of the primary references, as discussed above. Reconsideration and allowance is respectfully requested.

Claims 10 and 13 were rejected under 35 USC § 103(a) as being unpatentable over Takeda et al. (U.S. Patent No. 5,892,271) and Bickford et al. (U.S. Patent No. 4,862,322) as applied to claim 7 above, and further in view of admitted prior art (APA). Claims 10 and 13

include each limitation of their parent claim and are not obvious in view of the cited references for the reasons given above. Reconsideration and allowance is respectfully requested.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 359-3267 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18 day of January, 2005.

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